What is claimed is:

1. A semiconductor device comprising:

a first semiconductor region of a first conductivity type, defined by a first end surface, a second end surface opposing to the first end surface and a side boundary surface connecting the first and second end surfaces;

a second semiconductor region of the first conductivity type connected with said first semiconductor region at the second end surface;

a third semiconductor region of a second conductivity type connected with said first semiconductor region at the first end surface; and

a fourth semiconductor region having inner surface in contact with the side boundary surface and an impurity concentration lower than said first semiconductor region, configured such that the fourth semiconductor region surrounds said first semiconductor region, the fourth semiconductor region is disposed between the second and third semiconductor regions.

2. The semiconductor device of Claim 1, wherein said fourth semiconductor region has the first conductivity type.

3. The semiconductor device of Claim 1, wherein outer surface of said fourth semiconductor region serves as a chip outer-surface of the semiconductor device and the chip outer-surface is substantially orthogonal with the second end surface of said first semiconductor region.

4. The semiconductor device of Claim 1, wherein said fourth semiconductor region is made of a wafer cut from bulk crystal.

5. The semiconductor device of Claim 1, further comprising a first main electrode layer is formed on a bottom surface of said second semiconductor region.

6. The semiconductor device of Claim 5, wherein said first main electrode layer is contacted with said second semiconductor region, trough a first concavity formed at the bottom surface of said second semiconductor region.

7. The semiconductor device of Claim 1, further comprising a first main electrode layer, a part of the first main electrode layer is buried in a via hole penetrating through said second semiconductor region, configured such that the buried part of the first main electrode layer contacts with said first semiconductor region.

8. The semiconductor device of Claim 1, further comprising a second main electrode layer is formed on a top surface of said third semiconductor region.

9. The semiconductor device of Claim 8, wherein said second main electrode layer is contacted with said third semiconductor region, trough a second concavity formed at the top surface of said third semiconductor region.

10. A method of manufacturing a semiconductor device comprising:

preparing a semiconductor substrate defined by a first main surface a second main surface opposing to the first main surface;

forming a first semiconductor region by selectively doping first conductivity type impurity elements through a diffusion window disposed on the second main surface to a predetermined diffusion depth;

forming a second semiconductor region by doping the first conductivity type impurity elements through entire first main surface; and

forming a third semiconductor region by doping second conductivity type impurity elements through entire second main surface so as to form a pn junction with said first semiconductor region.

11. The manufacturing method of Claim 10, further comprising:

dividing the semiconductor substrate by cutting with planes substantially perpendicular to the first main surface so as to obtain a plurality of semiconductor chips, each formed into a rectangular parallelepiped shape.